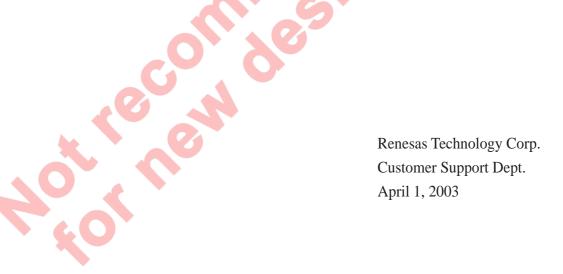
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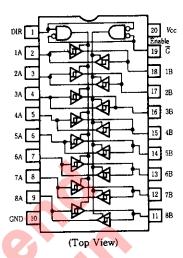
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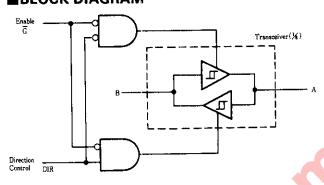
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This octal bus transceivers is designed for asynchronous two-way communication between data buses. The devices transmit data, from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so that the buses are effectively isolated.

PIN ARRANGEMENT



■BLOCK DIAGRAM



TRECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply voltage	Vcc	4.75	5.00	5.25	V
Output voltage	Von	\ _		5.5	V
Output current	IoL			48	mA
Operating temperature range	Topr	-20	25	75	ů

FUNCTION TABLE

Enable	Direction Control	Operation
Ğ	DIR	Operation
L	L	B data to A bus
L	Н	A data to B bus
Н	×	Isolation

Notes) H; high level, L; low level, X; irrelevant

ELECTRICAL CHARACTERISTICS $(Ta = -20 \sim +75^{\circ}C)$

Item	Symbol	Test Conditions		min	typ*	max	Unit
T 1	ViH			2.0	-	_	V
Input voltage	VIL			_	_	0.8	V
Hysteresis	$V_{T^{+}} - V_{T^{-}}$	$V_{CC} = 4.75 \text{V}$		0.2			V
Output current	Іон	$V_{CC} = 4.75 \text{V}, \ V_{IH} = 2 \text{V}, \ V_{IL} = 0.8$	V, Von=5.5V			100	μA
			$I_{DL} = 12 \text{mA}$			0.4	V
Output voltage	Voi	$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8 \text{V}$	Iot = 24 mA			0.5	V
		Iot. = 48			_	0.5	V
T .	Іін	$V_{CC} = 5.25 \text{V}, \ V_I = 2.7 \text{V}$				20	μA
Input current	IIL	$V_{CC} = 5.25 \text{V}, \ V_I = 0.4 \text{V}$			-	400	μA
A or B	1,	1/ 5 051/	V _I =5.5V			0.1	mA
DIR or G	$ I_{I}$	$V_{CC} = 5.25V$	$V_I = 7V$			0.1	mA
•	Іссн				48	70	mA
Supply current	Icc.	$V_{CC} = 5.25 \text{V}$, output open			62	90	mA
	Iccz				64	95	mA
Input clamp voltage	Vik	$V_{CC} = 4.75 \text{V}, I_{IN} = -18 \text{mA}$		-		-1.5	V

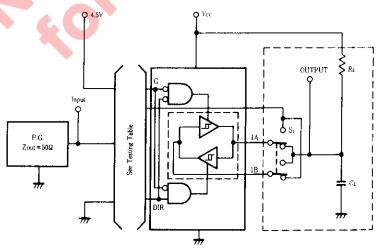
 $V_{CC} = 5V, Ta = 25^{\circ}C$

ESWITCHING CHARACTERISTICS ($V_{cc}=5V$, $T_a=25^{\circ}C$)

Item	Symbol	INPUT	OUTPUT	Test Conditions	min	typ	max	Unit
	tplн	A	В	$C_L = 45 \text{pF}, R_L = 667 \Omega$		17	25	ns
		В	A		_	17	25	ns
Propagation delay time		A	В			16	25	ns
	t _{PHL}	В	Α			16	25	ns
Output enable time	*n	Ğ	A	CL-45pr, RL-607 2		23	40	пs
	IPLR	$\bar{\mathbf{G}}$	В			25	40	ns
	four	Ğ	A			34	50	ns
	tphl	G	В			37	50	ns

TESTING METHOD

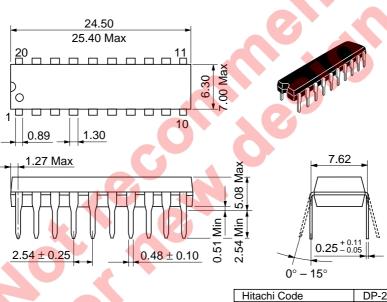
Test Circuit



Notes) 1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B, are identical to above load circuit.

- C_L includes probe and jig capacitance.
 S₁ is a input-output switch.

Unit: mm



Hitachi Code	DP-20N
JEDEC	_
EIAJ	Conforms
Weight (reference value)	1.26 g

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